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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,274	03/29/2001	Walter De Coster	859063.491	7289

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EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,274	COSTER ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 13-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 13-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *05 May 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figures 1 – 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on May 5, 2003 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 13 – 20 and 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the

relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not clear where in the originally filed specification support for "the first spacer having a concave surface" can be found. Further, it is not clear where in the originally filed specification support for "the spacer has a convex surface" can be found.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1 – 4, 7, 8 and 13 – 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Gambino et al. (USPAT 5994202, Gambino).

With regard to claim 1, Gambino discloses in figures 2a – 2i a method of forming an active area surrounded with an insulating area (18a – 18c) in a semiconductor substrate (12). Gambino discloses in figures 2a – 2i forming in the substrate a trench (17a – 17c) surrounding an active area (32a – 32d). Gambino discloses in figures 2a – 2i filling the trench with an insulating material (18a – 18c) to form an edge extending beyond a surface of the substrate at a periphery

of the active area. Gambino discloses in figures 2a – 2i forming a spacer (16) at a periphery of said edge. Gambino discloses in figures 2a – 2i and column 9, lines 10 – 26 implanting (19) a dopant of a first type (a type that modifies the conductivity of the substrate 10) only to provide a channel zone of a MOS transistor in the active area, whereby the implantation in an area located under the spacer is less deep than in the rest of the active area. Gambino discloses in figures 2a – 2g and column 9, lines 10 – 26 forming a conductive gate (35) on the active area after the implanting step without implanting any dopants of other than the first type in the active area prior to forming the conductive gate.

With regard to claim 2, Gambino discloses in figures 2a – 2i wherein the spacer has a substantially vertical edge with a thickness that thins down as the distance from said edge increases.

With regard to claim 3, Gambino discloses in figures 2a – 2i wherein the implantation step is followed by a step of removing the spacer prior to forming the conductive gate.

With regard to claim 4, Gambino discloses in figures 2a – 2i and column 9, lines 10 – 26 wherein the step of removing the spacer is followed by a step of implantation of another active area with a dopant of another conductivity type than that of the dopant.

With regard to claim 7, Gambino discloses in figures 2a – 2i and column 9, lines 1 – 5 wherein the spacer is made of silicon nitride.

With regard to claim 8, Gambino discloses in figures 2a – 2i and column 9, lines 1 – 5 wherein the spacer is made of polysilicon.

With regard to claim 13, Gambino discloses in figures 2a – 2i a method of forming a doped active area in a semiconductor substrate. Gambino discloses in figures 2a – 2i forming

first and second insulation areas on a surface of the substrate, the first and second insulation areas being spaced apart from each other and thereby defining a substrate region of the substrate between the first and second insulation areas, the substrate region having a first peripheral portion immediately adjacent to the first insulation area and a central portion spaced apart from the first insulation area. Gambino discloses in figures 2a – 2i forming a first spacer adjacent to the first insulation area and above the first peripheral portion of the substrate region. As far as the examiner can ascertain Gambino discloses the first spacer having a concave surface. Gambino discloses in figures 2a – 2i performing, after forming the first spacer, a first dopant implant into the substrate region to create the doped active area, the first spacer acting as a mask to allow dopants to extend deeper into the central portion that into the first peripheral portion.

With regard to claim 14, Gambino discloses in figures 2a – 2i wherein the substrate region has a second peripheral portion immediately adjacent to the second insulation area, the method further comprising forming a second spacer adjacent to the second insulation area and above the second peripheral portion of the substrate region, wherein performing the first dopant implant is executed after forming the second spacer, the second spacer acting as a mask to allow dopants to extend deeper into the central portion that into the second peripheral portion.

With regard to claim 15, Gambino discloses in figures 2a – 2i forming in the substrate first and second trenches on opposite sides of the substrate region, wherein forming the first and second insulation areas includes filling the trenches with insulating material and extending the insulating material to a level above a surface of the substrate region.

With regard to claim 16, Gambino discloses in figures 2a – 2i wherein the first dopant implant forms a first well that extends into the substrate region to a first level and the first and

second trenches extend into the substrate to a second level, the method further comprising performing a second dopant implant into the substrate region, thereby forming a second well that extends into the substrate region to the second level.

With regard to claim 17, Gambino discloses in figures 2a – 2i wherein the first spacer has a bell shape with a thickness that thins down as the distance from the first insulation area increases.

With regard to claim 18, further comprising: removing the first spacer after performing the first dopant implant; and depositing a first conductive layer (35) on the substrate region.

With regard to claim 19, Gambino discloses in figures 2a – 2i further comprising forming a protective coating (14) directly on the substrate region before forming the first spacer, the first spacer being formed on the protective coating.

With regard to claim 20, Gambino discloses in figures 2a – 2i and column 9, lines 1 – 5 wherein the first spacer is made of silicon nitride.

7. Claims 20 – 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Liao (USPAT 6235596, Liao).

With regard to claim 21, Liao discloses in figures 1 – 5 a method of forming a doped active area in a semiconductor substrate. Liao discloses in figures 1 – 5 forming first and second insulation areas (130) on a surface of the substrate, the first and second insulation areas being spaced apart from each other and thereby defining a substrate region (10) of the substrate between the first and second insulation areas, the substrate region having a first peripheral portion immediately adjacent to the first insulation area and a central portion spaced apart from

the first insulation area. Liao discloses in figures 1 – 5 forming a first spacer (150) adjacent to the first insulation area and above the first peripheral portion of the substrate region. Liao discloses in figures 1 – 5 performing, with the spacer positioned above the substrate, a high-energy first implant of first dopant type (a type that modifies the conductivity of the substrate) into the substrate region to create a well (160) that extends in the substrate at a bottom side of the first insulation area. Liao discloses in figures 1 – 5 performing with the spacer positioned above the substrate, a low-energy second implant (180) of the first dopant type into the substrate region to create the doped active area, the spacer acting as a mask to allow dopants of the second implant to extend deeper into the central portion than into the first peripheral portion.

With regard to claim 22, Liao discloses in figures 1 – 5 further comprising forming a conductive gate (190) on the active area after performing the first and second implants without implanting any dopants of other than the first dopant type in the active area prior to forming the conductive gate.

With regard to claim 23, as far as the examiner can ascertain Liao discloses wherein the spacer has a convex surface.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gambino as applied to claim 1 above, and further in view of Gardner et al. (USPAT 6077,748, Gardner).

With regard to claim 5, Gardner discloses in figures 2b – 2i a step of forming, at the surface of the active area, a protective coating (68). Gardner does not disclose forming the protective coating between the trench filling step and spacer forming step. Gardner discloses in figures 2b – 2i a step of forming, at the surface of the active area, a protective coating (68) between the trench filling step and spacer forming step. It would have been obvious to one of ordinary skill in the art to form the protective coating of Gardner in the process of Gambino in order to provide a fresh surface free of particles remaining after the nitride strip. This fresh surface ensures uniformity of the spacer layer resulting in good electrical properties as a result of the implantation steps.

With regard to claim 6, Gardner discloses in figures 2b – 2i and column 4, lines 26 – 37 wherein the protective coating results from the thermal growth of a thin silicon oxide layer at the surface of the substrate.

10. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liao as applied to claim 21 above, and further in view of Gambino.

It is not clear if Liao teaches planarizing top surfaces of the insulating areas after performing the second implant. Gambino discloses in figures 2a – 2g further comprising planarizing top surfaces of an insulating area after performing a second implant. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the

planarization step of Gambino in the method of Liao in order to provide improved step coverage during lithography steps for the formation of the gate in order to minimize line width variation.

Response to Arguments

11. Applicant's arguments filed May 5, 2003 have been fully considered but they are not persuasive.

12. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "without requiring two implant steps of dopants of opposite conductivity type") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
June 4, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800